UNITED STATES PATENT AND TRADEMARK OFFICE

A

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/964,010	09/26/2001	Matthew B. Haycock	884.455US1	1876

21186 7590 07/29/2005

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402-0938

EXAMINER	
CHEN, TSE W	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 07/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/964,010	HAYCOCK ET AL.	
	Examiner	Art Unit	
	Tse Chen	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10-22 and 31-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-22 and 31-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment dated May 23, 2005.

2. Claims 10-22 and 31-35 are presented for examination. Applicant has canceled claims 1-9 and 23-30.

Claim Objections

3. Claim 35 is objected to because of the following informalities: "a comparing a plurality of bits..." should be "comparing a plurality of bits..." Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 35 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted steps are: configuration processing necessary to produce the alignment of plurality of output bits provided at one of the output nodes with a plurality of output bits provided at other output nodes based on the rotation number that is used to rotate data held in a number of register cells of each of the register circuits. Without the necessary configuration processing, the plurality of output bits provided at the output nodes would not be aligned as the data held in the number of register cells of each of the register circuits would remain in the same relative position after the same number of rotations. However, in the interest of compact prosecution, prior art is still applied.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 31 and 33 are rejected under 35 U.S.C. 102(b) as being anticipated by Wood et al., US Patent 4246656, hereinafter Wood

8. In re claim 31, Wood discloses a method comprising [fig.1; col.4, l.59 – col.5, l.53]:

- Receiving a plurality of input bits at a plurality of input nodes [42, 44] of a plurality of register circuits [shift register 50/mux 54 and shift register 52/mux 56 constitutes register circuits].
- Providing a plurality of output bits at a plurality of output nodes [72, 74] of the register circuits.
- Performing a logic function [compare] on a plurality of bits held by the register circuits to produce a rotation number [three bit errors require advancing or retreating in rotation number of three bits in order to find correlation].
- Aligning a plurality of output bits provided at one of the output nodes with a plurality of output bits provided at other output nodes, based on the rotation number, when the plurality of input bits received at the input nodes are misaligned by at least one bit time interval [correlating and selecting appropriate mux line based on the advancing or retreating rotation aligns the output bits].

9. As to claim 33, Wood discloses, wherein each of the register circuits further including a select circuit [54, 56] connected to a subset of the number of register cells through a number of select lines [62, 64].

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Taya et al., US Patent 5778214, hereinafter Taya, in view of Yamamoto et al., Japanese Publication 06-120937, hereinafter Yamamoto.

12. In re claim 10, Taya discloses an integrated circuit [pattern detection circuit 2] comprising:

- A plurality of input nodes [fig.2; inputs to the registers].
- A plurality of output nodes [fig.2; outputs from sync pattern check circuits].
- A plurality of register circuits [shift registers], each of the register circuits being connected between one of the input nodes and one of the output nodes to receive a plurality of input bits at one of the input nodes and to provide at one of the output nodes a plurality of output bits based on the plurality of input bits [fig.2; shift registers connected between input nodes and output nodes in the broadest interpretation – e.g., node being a point in the data path before or after the shift register].

13. Taya did not discuss the details of a logic circuit or controller.

14. Yamamoto discloses an integrated circuit [abstract, accompanying figure] comprising:

- A logic circuit [comparison means 3] connected to the register circuits [shift registers and storage means] to perform a logic function [compare] on a plurality of input bits [signal] held by one of the register circuits [shift register 2] among the plurality of the register circuits with the plurality of input bits held by the other register circuits [storage means 4] among the plurality of register circuits [paragraph 0011].
- A controller [control means 5] to configure the register circuits based on a result from the logic function [compare] of the logic circuit to align the plurality of output bits provided by one output node [shift register 2 bits to comparison means 3] with a plurality of output bits provided by other output nodes [storage means 4 to comparison means 3] when the plurality of input bits received at one of the input nodes [shift register 2] are misaligned with the plurality of input bits received at the other input nodes [storage means 4] by one or more bit time intervals [paragraphs 0012-0013; when bits in 2 and 4 do not align, circuit configures by continually shifting and comparing bits until alignment].

15. It would have been obvious to one of ordinary skill in the art, having the teachings of Taya and Yamamoto before him at the time the invention was made, to modify the system taught by Taya to include the logic circuit and controller taught by Yamamoto, in order to obtain the claimed integrated circuit with simplicity and reduction in current consumption [Yamamoto: abstract]. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to synchronize with simplicity and reduction in current consumption.

16. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Taya and Yamamoto as applied to claim 10 above, and further in view of Fukuoka, US Patent 6467063.

17. Taya and Yamamoto disclose each an every limitation of the claim as discussed above in reference to claim 10. Taya and Yamamoto did not discuss the details regarding the number of register cells as related to the maximum number of bit timer intervals of misalignment.

18. Fukuoka discloses a circuit [Reed Solomon coding apparatus] comprising:

- Register circuits [90-97] that include a number of register cells, wherein the number of register cells equals 2M-1 [2s-1], where M [s] is a maximum number of bit time intervals of misalignment [maximum number of errors] [col.14, ll.48-60].

19. It would have been obvious to one of ordinary skill in the art, having the teachings of Fukuoka, Taya and Yamamoto before him at the time the invention was made, to modify the system taught by Taya and Yamamoto to include the register circuits taught by Fukuoka, in order to obtain the claimed integrated circuit wherein each of the register circuits includes a number of register cells, wherein the number of register cells equals 2M-1, where M is a maximum number of bits time intervals of misalignment of a parallel bus that connects to the integrated circuit. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to correct multiple errors in a processing system [Fukuoka: col.1, ll.6-15].

20. Claims 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukuoka, Taya and Yamamoto as applied to claim 11 above, and further in view of Moriwaki et al., US Patent 6753872, hereinafter Moriwaki.

21. In re claim 12, Fukuoka, Taya and Yamamoto disclose each an every limitation of the claim as discussed above in reference to claim 11. Fukuoka, Taya and Yamamoto did not discuss the details of a select circuit.

22. Moriwaki discloses a system [rendering processing system] comprising register circuits that include:

- A select circuit [selector 51] connected to a subset of the number of register cells [set of 50-x registers] through a number of select lines [24b] [fig.5; col.9, ll.7-54].

23. It would have been obvious to one of ordinary skill in the art, having the teachings of Moriwaki, Fukuoka, Taya and Yamamoto before him at the time the invention was made, to modify the system taught by Fukuoka, Taya and Yamamoto to include the select circuit taught by Moriwaki, in order to obtain the claimed integrated circuit wherein each of the register circuits further includes a select circuit connected to a subset of the number of register cells through a number of select lines. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to select and process particular sets of data bits [Moriwaki: col.9, ll.24-42].

24. As to claim 13, Moriwaki, Fukuoka, Taya and Yamamoto discloses each an every limitation of the claim as discussed above in reference to claim 12. It would have been obvious to one of ordinary skill in the art, having the teachings of Moriwaki, Fukuoka, Taya and Yamamoto before him at the time the invention was made, to modify the system taught by Fukuoka, Taya and Yamamoto to include the select lines taught by Moriwaki, in order to obtain the claimed integrated circuit wherein the number of select lines equals a maximum number bit time intervals of misalignment of a parallel bus that connects to the integrated circuit. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to select and process particular sets of data bits [Moriwaki: col.9, ll.24-42; associate select lines with M since there's no need to further process bits greater than the maximum error].

25. Claims 14 and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wood, in view of Yamamoto and Fukuoka.

26. In re claim 14, Wood discloses an integrated circuit [diversity switch correlation circuit] comprising [fig.1; col.4, l.59 – col.5, l.53]:

- A plurality of input nodes to receive a plurality of input bits [42, 44].
- A plurality of output nodes to provide a plurality of output bits [72, 74].
- A plurality of register circuits [50/54 and 52/56], each of the register circuits being connected between one of the input nodes and one of the output nodes [e.g., 50/54 between 42 and 72], each of the register circuits including a number of register cells [8 bits], each of the register circuits further including a select circuit [54, 56] connected to a subset of the number of register cells through a number of select lines [62, 64].
- A logic circuit [66, 58, 60 with associated circuitries] connected to the register circuits to perform a logic function [compare] on a plurality of bits held by the register circuits, wherein the logic circuit includes:
    - A calculation unit to perform the logic function on a plurality of bits [66 compares the bits from the different data streams to detect correlation].
    - A plurality of memory units to store results from the logic function [58, 60 stores the uncorrelated results from 66].
    - A counter to count values stored in the memory units [58, 60 counts uncorrelated results from 66].

- A detect logic to determine results from the counter and to generate a rotation number [58, 56 determines the rotation number to advance or retreat by bits in order to align].

- A controller to configure the register circuits based on a result from the logic circuit to align the plurality of output bits provided by one output node with a plurality of output bits provided by other output nodes when the plurality of input bits received at the input nodes are misaligned by one or more bit time intervals [58 configures 54 to select appropriate line for aligning the data streams].

27. Wood did not discuss the details involved with rotating the data held in the number of register cells or the details regarding the number of register cells as related to the maximum number of bit timer intervals of misalignment.

28. Yamamoto discloses an integrated circuit [abstract, accompanying figure] comprising:

- A detect logic [5] to generate a rotation number [shift 1 bit], the rotation number being used to rotate data held in the number of register cells [paragraphs 0012-0013; when bits in 2 and 4 do not align, circuit configures by continually shifting and comparing bits until alignment].

29. It would have been obvious to one of ordinary skill in the art, having the teachings of Wood and Yamamoto before him at the time the invention was made, to modify the system taught by Wood to include the logic circuit and controller taught by Yamamoto, in order to obtain the claimed integrated circuit comprising a detect logic to determine results from the counter and to generate a rotation number, the rotation number being used to rotate data held in the number of register cells. One of ordinary skill in the art would have been motivated to make

such a combination as it provides a very well known way to access particular bits of data [rotating] while synchronizing data streams with simplicity and reduction in current consumption [Yamamoto: abstract].

30. Fukuoka discloses a circuit [Reed Solomon coding apparatus] comprising:

- Register circuits [90-97] that include a number of register cells, wherein the number of register cells equals 2M-1 [2s-1], where M [s] is a maximum number of bit time intervals of misalignment [maximum number of errors] [col.14, ll.48-60].

31. It would have been obvious to one of ordinary skill in the art, having the teachings of Fukuoka and Wood before him at the time the invention was made, to modify the system taught by Wood to include the register circuits taught by Fukuoka, in order to obtain the claimed integrated circuit wherein each of the register circuits includes a number of register cells, wherein the number of register cells equals 2M-1, where M is a maximum number of bits time intervals of misalignment of a parallel bus that connects to the integrated circuit. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to correct multiple errors in a processing system [Fukuoka: col.1, ll.6-15].

32. Furthermore, it would have been obvious to one of ordinary skill in the art, to further modify the system taught by Fukuoka and Wood in order to obtain the claimed integrated circuit wherein the number of select lines equals a maximum number bit time intervals of misalignment of a parallel bus that connects to the integrated circuit. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to select and process particular sets of data bits [Wood: col.3, ll.40-55; associate select lines with M since there's no need to further process bits greater than the maximum error].

33. As to claim 16, Examiner hereby takes Official Notice that it is well known in the art to arrange memory units in rows and columns, wherein the memory units in the same row form a shift register.

34. As to claim 17, Wood discloses, wherein the counter [58, 60] includes a plurality of counter memory units [2 units], each of the counter memory units being connected to one shift register [58/50 and 60/52].

35. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Taya and Yamamoto as applied to claim 10 above, and further in view of Jaquette, US Patent 5737371.

36. Taya and Yamamoto disclose each an every limitation of the claim as discussed above in reference to claim 10. Taya and Yamamoto did not discuss the details of the logic circuit.

37. Jaquette discloses a logic circuit that performs an OR function [col.5, l.54 – col.7, l.15].

38. It would have been obvious to one of ordinary skill in the art, having the teachings of Jaquette, Taya and Yamamoto before him at the time the invention was made, to use the logic circuit with the OR function taught by Jaquette for the integrated circuit disclosed by Taya and Yamamoto as the logic circuit with the OR function taught by Jaquette is a very well known function suitable for use with the integrated circuit of Taya and Yamamoto. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to validate certain conditions with a well-known logic function [Jaquette: col.5, l.54 – col.6, l.9].

39. Claims 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moriwaki in view of Grondalski, US Patent 6108763 and Wood.

40. In re claim 18, Moriwaki discloses a system [rendering processing system] comprising:

- A parallel bus [internal data bus 15] including a plurality of bus lines to carry a plurality of bits on each of the bus lines [fig.5; col.9, ll.7-23].
- A first integrated circuit [data transfer circuit 12] including a plurality of register circuits [50-1 to 50-64], each of the register circuits being connected to one of the bus lines [col.9, ll.7-23].
- Each of the register circuits including:
- A register [set of three 24-bits 50-x registers combined for 64 bits] connected to an input node [inherently, an input node in the broadest interpretation is at the other end of the bus], the register including a plurality of register cells [set of 50-x registers] [col.9, ll.7-41].
- A select circuit [selector 51] connected to a subset of the number of register cells through a number of select lines [24b], the select circuit including an output node [switch circuit 52] [fig.5; col.9, ll.24-54].
- A controller [memory control circuit 4] connected to the select circuit and the register cells to configure the register cells to select the select lines to be a part of a conductive path connected between the input node and the select circuit output node [col.9, l.24 – col.10, l.17; selector selects the 64 bits to be connected].

41. Moriwaki did not disclose explicitly that the registers are to be shift registers, that only one of the select lines is to be selected, or that each of the register circuits are to have their individual select circuits.

42. Grondalski discloses a system [fig.4] comprising:

- A shift register [52] including a plurality of register cells [col.19, ll.40-54].

- A controller [issues the sel cell signal] connected to the register cells to configure the register cells to select only one of the select lines [col.21, ll.12-56; sel cell signal corresponding to sel8 with associated transistors for particular register cell].

43. It would have been obvious to one of ordinary skill in the art, having the teachings of Moriwaki and Grondalski before him at the time the invention was made, to use the shift register taught by Grondalski for the system disclosed by Moriwaki as the shift register taught by Grondalski is a well known device suitable for use as the register of Moriwaki. One of ordinary skill in the art would have been motivated to make such a combination as it provides a well-known way to manipulate data in a processing system [Grondalski: col.19, l.40 – col.20, l.22].

44. Wood discloses a system comprising [fig.1; col.4, l.59 – col.5, l.53]:

- A first integrated circuit [diversity switch correlation circuit] including a plurality register circuits [50/54 and 52/56], each of the register circuits including:
    - A select circuit [e.g., 54] connected to a subset of the number of register cells through a number of select lines [e.g., 62], the select circuit including an output node [e.g., 72].

45. It would have been obvious to one of ordinary skill in the art, having the teachings of Moriwaki and Wood before him at the time the invention was made, to modify the system taught by Moriwaki to include the teachings of Wood in order to obtain the claimed integrated circuit wherein each of the register circuits include an individual select circuit. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to select and process particular sets of data bits [Wood: col.3, ll.40-55].

46. As to claim 19, Moriwaki discloses the system comprising a second integrated circuit [rendering operation circuit 2] connected to the parallel bus [fig.5].

47. As to claim 20, Moriwaki discloses the system wherein the parallel bus is formed on a circuit board, and the first and second integrated circuits are located in the circuit board [col.6, l.64 – col.7, l.22; on board wiring of bus].

48. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wood, Moriwaki and Grondalski as applied to claim 19 above, and further in view of Barnsley et al., US Patent 5430812, hereinafter Barnsley.

49. Wood, Moriwaki and Grondalski disclose each an every limitation of the claim as discussed above in reference to claim 19. Wood, Moriwaki and Grondalski did not discuss separate circuit board configuration.

50. Barnsley discloses a system [fig.5; digital image data compression apparatus] comprising:

- A first circuit board [pc 112], wherein the parallel bus [AT bus 118] is formed on the first circuit board and a first integrated circuit [80386] is located on the first circuit board [col.4, ll.53-68].
- A second circuit board [110], wherein a second integrated circuit [fractal transform chips] is located on the second circuit board, the second circuit board being inserted into a bus slot that connects to the parallel bus [col.4, ll.53-68].

51. It would have been obvious to one of ordinary skill in the art, having the teachings of Wood, Barnsley, Moriwaki and Grondalski before him at the time the invention was made, to use the circuit board configuration taught by Barnsley for the system disclosed by Wood, Moriwaki

and Grondalski as the circuit board configuration taught by Barnsley is a well known configuration suitable for use with the system of Wood, Moriwaki and Grondalski. One of ordinary skill in the art would have been motivated to make such a combination as it provides a well-known way to interconnect various parts in a processing system [Barnsley: col.4, ll.53-68].

52. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wood, Moriwaki and Grondalski as applied to claim 19 above, and further in view of Frisch et al., US Patent 4707834, hereinafter Frisch.

53. Wood, Moriwaki and Grondalski disclose each an every limitation of the claim as discussed above in reference to claim 19. Wood, Moriwaki and Grondalski did not discuss separate circuit board configuration.

54. Frisch discloses a system [instrument system] comprising a first and second integrated circuit [instruments 12] that are located on separate circuit boards, and the parallel bus [26] is not formed on the first or second circuit boards [col.4, ll.28-58].

55. It would have been obvious to one of ordinary skill in the art, having the teachings of Wood, Frisch, Moriwaki and Grondalski before him at the time the invention was made, to use the circuit board configuration taught by Frisch for the system disclosed by Wood, Moriwaki and Grondalski as the circuit board configuration taught by Frisch is a well known configuration suitable for use with the system of Wood, Moriwaki and Grondalski. One of ordinary skill in the art would have been motivated to make such a combination as it provides a well-known way to interconnect various parts in a processing system [Frisch: col.4, ll.28-58].

56. Claims 32 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wood as applied to claim 31 above, and further in view of Fukuoka.

57. In re claim 32, Wood discloses each and every limitation of the claim as discussed above in reference to claim 31. Wood did not discuss the details regarding the number of register cells as related to the maximum number of bit timer intervals of misalignment.

58. Fukuoka discloses a circuit [Reed Solomon coding apparatus] comprising:

- Register circuits [90-97] that include a number of register cells, wherein the number of register cells equals 2M-1 [2s-1], where M [s] is a maximum number of bit time intervals of misalignment [maximum number of errors] [col.14, ll.48-60].

59. It would have been obvious to one of ordinary skill in the art, having the teachings of Fukuoka and Wood before him at the time the invention was made, to modify the system taught by Wood to include the register circuits taught by Fukuoka, in order to obtain the claimed integrated circuit wherein each of the register circuits includes a number of register cells, wherein the number of register cells equals 2M-1, where M is a maximum number of bits time intervals of misalignment of a parallel bus that connects to the integrated circuit. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to correct multiple errors in a processing system [Fukuoka: col.1, ll.6-15].

60. As to claim 34, it would have been obvious to one of ordinary skill in the art, to further modify the system taught by Fukuoka and Wood in order to obtain the claimed integrated circuit wherein the number of select lines equals a maximum number bit time intervals of misalignment of a parallel bus that connects to the integrated circuit. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to select and process particular sets of data bits [Wood: col.3, ll.40-55; associate select lines with M since there's no need to further process bits greater than the maximum error].

61. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wood as applied to claim 31 above, and further in view of Yamamoto.

62. Wood discloses each and every limitation of the claim as discussed above in reference to claim 31. In particular, Wood discloses, wherein the performing the logic function includes [fig.1; col.4, l.59 – col.5, l.53]:

- Comparing a plurality of bits among the input nodes to produce a comparison result [66 compares the bits from the different data streams to detect correlation].
- Storing the comparison result in memory units [58, 60 stores the uncorrelated results from 66].
- Counting values stored in the memory units [58, 60 counts uncorrelated results from 66].
- Determining results from the counting to generate the rotation number [58, 56 determines the rotation number to advance or retreat by bits in order to align].

63. Wood did not discuss the details involved with rotating the data held in the number of register cells.

64. Yamamoto discloses an integrated circuit [abstract, accompanying figure] comprising:

- A detect logic [5] to generate a rotation number [shift 1 bit], the rotation number being used to rotate data held in a number of register cells of each of the register circuits [shift registers 1 and 2] [paragraphs 0012-0013; when bits in 2 and 4 do not align, circuit configures by continually shifting and comparing bits until alignment].

65. It would have been obvious to one of ordinary skill in the art, having the teachings of Wood and Yamamoto before him at the time the invention was made, to modify the system taught by Wood to include the logic circuit and controller taught by Yamamoto, in order to

obtain the claimed integrated circuit comprising a detect logic to determine results from the counter and to generate a rotation number, the rotation number being used to rotate data held in the number of register cells of each of the register circuits [Wood aligns bits of Yamamoto rotation which produces same relative position with advancing/retreating mux select line]. One of ordinary skill in the art would have been motivated to make such a combination as it provides a very well known way to access particular bits of data [rotating] while synchronizing data streams with simplicity and reduction in current consumption [Yamamoto: abstract].

Response to Arguments

66. Applicant's arguments filed May 23, 2005 have been fully considered but they are not persuasive.

67. In re claim 31, Applicant was not able to find in Wood "all of the things recited". Examiner respectfully submits that Wood discloses each and every limitation of the method comprising: receiving a plurality of input bits at a plurality of input nodes [42, 44] of a plurality of register circuits [shift register 50/mux 54 and shift register 52/mux 56 constitutes register circuits]; providing a plurality of output bits at a plurality of output nodes [72, 74] of the register circuits; performing a logic function [compare] on a plurality of bits held by the register circuits to produce a rotation number [three bit errors require advancing or retreating in rotation number of three bits in order to find correlation]; and aligning a plurality of output bits provided at one of the output nodes with a plurality of output bits provided at other output nodes when the plurality of input bits received at the input nodes are misaligned by at least one bit time interval [correlating and selecting appropriate mux line aligns the output bits] [fig.1; col.4, l.59 – col.5, l.53].

68. In re claim 10, Applicant alleges that "Taya teaches, in fig.2, ... shows that all of the input nodes of shift registers 22a, 22b, and 22c receive data from the same node (output node of SW12a)". Examiner disagrees and submits that fig.2 also shows output nodes of SW12b-n. Applicant was not able to find in Taya "a plurality of register circuits... to provide at one of the output nodes a plurality of output bits based on the plurality of input bits". Examiner reminds Applicant that bits do not have to be high in order to be considered bits. Applicant was not able find in Yamamoto "that each of the shift register 2 and storage means 4 of Yamamoto is connected between an input node and an output node to receive a plurality of input bits and to provide at the output node a plurality of output bits based on the plurality of inputs bits". Examiner submits that the shift registers and storage means of Yamamoto inherently requires the cited limitations in order to have the input/output capabilities taught. Moreover, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). In the instant case, Examiner reminds Applicant that the rejection was based on a combination where Taya was specifically cited for those teachings. Applicant was not able to find in Yamamoto " a logic circuit connected to the register circuits to perform a logic function on the plurality of input bits held by one of the register circuits among the plurality of the register circuits with the plurality of input bits held by the other register circuits among the plurality of register circuits". Examiner reminds Applicant that the number two is considered to be a plurality. Applicant was not able to find in Yamamoto "a showing or a fair suggestion that the control means 5 of Yamamoto is used to configure both shift register 2 and storage means 4..." Examiner reminds Applicant that claim 10 recites that the

controller of claim 10 is to "configure the register circuits..." Applicant was not able to find in Taya and Yamamoto, "either individual or in combination, a fair suggestion or motivation to combine Taya and Yamamoto, as proposed by the Office Action..." Examiner was not able to find in Applicant's arguments any support for Applicant's allegation and invites Applicant to read/review the rejection to note that the motivation was explicitly cited from Yamamoto to provide a way to synchronize with simplicity and reduction in current consumption.

69. In re claim 14, Applicant was not able to find in Wood "each of the register circuits further including a select circuit connected to a subset of the number of register cells through a number of select lines". Examiner disagrees and submits that Applicant appears to have evinced a misreading of "lines 62" instead of "line 62".

70. In re claim 18, Applicant was not able to find in Moriwaki "a showing or a fair suggestion that 'each' of the register circuits... includes a shift register and a select circuit... a select circuit connected to a subset of the number of register cells through a number of select lines". Examiner again submits that one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references and reminds Applicant that the rejection was based on a combination of Moriwaki, Grondalski and Wood to teach each and every limitation. Applicant was not able to find in Wood "each of the register circuits further including a select circuit connected to a subset of the number of register cells through a number of select lines". Examiner reminds Applicant that line 62 is not a plurality. Applicant was not able to find in Moriwaki, Grondalski and Wood, "either individual or in combination, a fair suggestion or motivation to combine Moriwaki, Grondalski and Wood, as proposed by the Office Action..." Examiner was not able to find in Applicant's arguments any support for Applicant's

allegation and invites Applicant to read/review the rejection to note that the motivation was explicitly cited for the combination.

71. All other claims were not argued separately.

Conclusion

72. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tse Chen
July 21, 2005

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100